

Electromigration Failure Prediction and Reliability Evaluation of Solder Bumps for FCBGA Package

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Electromigration (EM) in solder joints under high current density has become a critical reliability issue for the future high density microelectronic packaging. A practical method of atomic density integral (ADI) for predicting solder bump electromigration reliability is proposed in this paper. The driving forces in electromigration include electron wind force, stress gradient, temperature gradient as well as atomic density gradient. The electromigration simulation is performed on **flip chip ball grid array** (FCBGA) package based on ADI method, and the simulation results for void generation and time to failure (TTF) have a reasonably good correlation with the testing results. Orthogonal experimental design has been used to evaluate the effect of design parameters on TTF of electromigration. Based on this study, some practical recommendations are made to optimize the package design and improve the solder bump electromigration reliability.

Key words: electromigration, atomic density integral method, time to failure, orthogonal experimental design.

1. INTRODUCTION

In order to minimize the integrated circuits (IC), the choice of the flip-chip (FC) package is a solution, and the products of FC ball grid array (FCBGA) can meet the demands for high performance ICs, such as microprocessors and CPU [1]. As electronics industry continues to push for high performance and the miniaturization of electronic devices, the demand for high current density may cause electromigration failures in solder bumps of FCBGA package [2]. Electromigration is the diffusion controlled mass transfer phenomenon in metallization structures stressed with high electrical current density leading to accumulation of vacancies and atoms creating voids and hillocks. Whereas voids result in open circuit or increased line resistance that can cause circuit functional failure, hillock formation results in short circuit. Nowadays, EM has become one of the most significant threats to interconnect reliability in power electronic packages [3].

In engineering practice, Black's equation [4] is commonly used to predict time to failure of Al or Cu thin films in very-large-scale-integration (VLSI) interconnect under high current density. As an empirical equation, Black's equation is not accurate enough to evaluate the reliability or unable to reasonably simulate the failure due to void formation because it regards current density as a sole factor to induce electromigration. In addition, Black's equation assumes that the current density in aluminum is constant, which is also not true in solder bumps in which current density varies in different location. In fact, the electromigration failure mechanism in solder balls is distinctly different from that in Al or Cu interconnects [5, 6].

Tu, Basaran and their co-workers [7–9] have conducted many theoretical and experimental studies and reviews of solder bump electromigration failure mechanisms. According to their work and JEDEC standard JEP154, the failure phenomenon of electromigration was mostly found inside the solder joint which is adjacent to the under bump metallization (UBM) layer. Due to the unique geometry of a flip chip, current crowding occurs at the contact interface between the solder bump and the UBM. The current crowding and the high temperature at the contact interface between the solder bump and the UBM causes the formation of voids [10]. Except current crowding, there are also many other factors which will influence electromigration failure of solder bump, such as temperature, solder material and also package design. As the chip size shrinks, one challenge we face is how to design a robust package to reduce the electromigration failure and to obtain the longer TTF in an optimized solution.

In this paper, a practical method of atomic density integral (ADI) [11] is used to predict the electromigration failure of solder bumps in FCBGA package. The simulation results give the void generation and TTF of solder bump. In order to better understand how package structure and material affect the TTF of bump, further simulations have been performed by changing the geometry parameter of UBM, solder bump, heat spreader stiffener ring shape and also solder material. Then, orthogonal experimental design is used to evaluate the effect of design parameters on TTF. Finally, some recommendations are made for designing FCBGA package.

2. BASIC EQUATIONS FOR ELECTROMIGRATION

Electromigration is a diffusion controlled mass transport process in an interconnect structure. The time-dependent evolution equation of the local atomic density caused by an applied current is the mass balance (continuity) equation,

$$(2.1) \quad \nabla \cdot \mathbf{q} + \frac{\partial c}{\partial t} = 0,$$

where c is the normalized atomic density (NAD), $c = C/C_0$, C is the actual atomic density and C_0 is the initial (equilibrium state) atomic density in the absence of a stress field, t is the time and \mathbf{q} is the total normalized atomic flux.

The driving forces of atomic flux may include electron wind, temperature gradient, hydrostatic stress gradient and atomic density gradient; thus,

$$(2.2) \quad \mathbf{q} = \mathbf{q}_{Ew} + \mathbf{q}_{Th} + \mathbf{q}_S + \mathbf{q}_C = \frac{cD}{k_B T} e Z^* \mathbf{j} \rho - \frac{cD}{k_B T} Q^* \frac{\nabla T}{T} \\ - \frac{cD}{k_B T} \Omega \nabla \sigma_m - D \nabla c = c \cdot \mathbf{F}(\nabla T, \nabla \sigma_m, \mathbf{j}, \dots) - D \nabla c,$$

where k is Boltzmann's constant, e is the electronic charge, Z^* is the effective charge which is determined experimentally, T is the absolute temperature, ρ is the resistivity which is calculated as $\rho = \rho_0 (1 + \alpha(T - T_0))$, where α is the temperature coefficient of the metallic material, ρ_0 is the resistivity at T_0 , \mathbf{j} is the current density vector, Q^* is the heat of transport, Ω is the atomic volume, $\sigma_m = (\sigma_1 + \sigma_2 + \sigma_3)/3$ is the local hydrostatic stress, where $\sigma_1, \sigma_2, \sigma_3$ are the components of principal stress, D is the effective atom diffusivity, $D = D_0 \exp(-E_a/kT)$, where E_a is the activation energy, D_0 is the effective thermally activated diffusion coefficient.

For the EM evolution equation (Eq. (2.1)) on any enclosed domain V with the corresponding boundary Γ , the atomic flux boundary conditions of a metal interconnects can be expressed as

$$(2.3) \quad \mathbf{q} \cdot \mathbf{n} = q_0 \quad \text{on } \Gamma.$$

For blocking boundary condition,

$$(2.4) \quad q_0 = 0 \quad \text{on } \Gamma.$$

At the initial time, the normalized atomic density is assumed to be

$$(2.5) \quad c_0 = 1.$$

The above equations and boundary conditions constitute the boundary value problem that governs the atomic transport during EM. This boundary value problem must be solved accurately in order to adequately describe the continuous atom redistribution and to capture the realistic kinetics of void nucleation and growth as a function of the interconnect architecture, segment geometry, material properties and stress conditions.

3. ELECTROMIGRATION EVOLUTION METHOD

3.1. Atomic density integral algorithm

In general, atom redistribution, caused by kinds of EM driving forces, tends to bring the atomic system to quasiequilibrium (steady state). Depending on the particular solder bump geometry, material properties and applied electrical current, voids may be nucleated somewhere at the interface of UBM and solder bump. The nucleated void affects current density, temperature and mechanical stress distributions around the void; hence, it changes the local atomic fluxes in the void vicinity and leads to further void evolution.

Equation (2.1) describes the atom density evolution at any point of the considered segment characterized by the given current density \mathbf{j} , T , gradients of temperature and stress. Thus, to obtain a complete solution of the problem, we should determine in coupled manner the evolution of the current, temperature and stress distributions in the considered segment, caused by continuous atom density redistribution. We assume that the establishment of a new equilibrium in the current, temperature and stress distributions is immediate, but the process of atom migration is slow. Therefore, we can obtain the current, temperature and stress by the steady-state solutions. After we obtain the current, temperature, stress and atomic density distribution in an incremental step, the atomic density redistribution needs to be solved based on Eq. (2.1) in the next step.

In the finite element method, we seek an approximation solution for Eq. (2.1) to develop a new local simulation algorithm for the local atomic density in a solder bump. The first step is to multiply the time-dependent EM evolution equation with a weighted residual function w and integrate over the enclosed domain V based on the vector identity by applying the Gauss-Ostrogradsky divergence theorem to the product of the scalar function w and the atomic flux vector field:

$$(3.1) \quad \int_V w(\nabla \cdot \mathbf{q} + \dot{c}) dV = \int_V w\dot{c} dV + \int_V w \cdot (\nabla \cdot \mathbf{q}) dV \\ = \int_V w\dot{c} dV - \int_V \frac{\partial w}{\partial \mathbf{n}} \cdot \mathbf{q} dV + \int_\Gamma w \cdot (\mathbf{q} \cdot \mathbf{n}) d\Gamma = 0.$$

From Eq. (3.1) with considering the atomic flux boundary condition of Eq. (2.3),

$$(3.2) \quad \int_V w\dot{c} dV - \int_V \frac{\partial w}{\partial \mathbf{n}} \cdot \mathbf{q} dV = - \int_\Gamma wq_0 d\Gamma.$$

Next, we assume that

$$c = \sum_{j=1}^n \psi_j c^j, \quad \dot{c} = \sum_{j=1}^n \psi_j \dot{c}^j$$

and $w = \psi_i$ (for Galerkin method), where ψ_i is the shape function of the element. After element discretization, the matrix form of Eq. (3.2) can be written as

$$(3.3) \quad [\mathbf{M}] \{\dot{c}\} + [\mathbf{K}] \{c\} = \{\mathbf{Y}\},$$

where the mass matrix $[\mathbf{M}]$ is independent of time, the stiffness matrix $[\mathbf{K}]$ will remain constant in an incremental step where we assume that the current density \mathbf{j} and the local hydrostatic stress σ_m are not varied (i.e., both are constants) in the current incremental step, $\{\mathbf{Y}\}$ is the known term.

For an eight-node element e with volume V_e , mass matrix $[\mathbf{M}]$ and stiffness matrix $[\mathbf{K}]$ can be discretized as

$$(3.4) \quad [\mathbf{M}]_{ij}^e = \int_{V_e} \psi_i \psi_j dV_e = \sum_{k=1}^8 \psi_i(\xi_k, \eta_k, \zeta_k) \psi_j(\xi_k, \eta_k, \zeta_k) J_k w_k,$$

$$[\mathbf{K}]_{ij}^e = \int_{V_e} \left[- \left(\frac{\partial \psi_i}{\partial \mathbf{n}} \cdot \mathbf{F} \right) \psi_j + D \frac{\partial \psi_i}{\partial \mathbf{n}} \cdot \nabla \psi_j \right] dV_e,$$

where $[\mathbf{M}]_{ij}^e$ and $[\mathbf{K}]_{ij}^e$ are discretized forms of mass matrix $[\mathbf{M}]$ and stiffness matrix $[\mathbf{K}]$ respectively, ψ_i and ψ_j are shape function.

Furthermore, $[\mathbf{K}]_{ij}^e$ can be described as

$$(3.5) \quad [\mathbf{K}]_{ij}^e = \int_{V_e} \left[- \left(\frac{\partial \psi_i}{\partial \mathbf{n}} \cdot \mathbf{F} \right) \psi_j + D \frac{\partial \psi_i}{\partial \mathbf{n}} \cdot \nabla \psi_j \right] dV_e$$

$$= \int_{V_e} \left[- \left(\frac{\partial \psi_i}{\partial x} F_x + \frac{\partial \psi_i}{\partial y} F_y + \frac{\partial \psi_i}{\partial z} F_z \right) \psi_j \right.$$

$$\left. + D \left(\frac{\partial \psi_i}{\partial x} \cdot \frac{\partial \psi_j}{\partial x} + \frac{\partial \psi_i}{\partial y} \cdot \frac{\partial \psi_j}{\partial y} + \frac{\partial \psi_i}{\partial z} \cdot \frac{\partial \psi_j}{\partial z} \right) \right] dV_e$$

$$= \int_{V_e} [-G + H] dV_e = \sum_{k=1}^8 [-G(\xi_k, \eta_k, \zeta_k) + H(\xi_k, \eta_k, \zeta_k)] J(\xi_k, \eta_k, \zeta_k) W_k,$$

where

$$F_x = \frac{D}{kT} Z^* e \rho j_x - \frac{D}{kT} Q^* \frac{1}{T} \frac{\partial T}{\partial x} - \frac{D}{kT} \Omega \frac{\partial \sigma_m}{\partial x},$$

$$\begin{aligned}
F_y &= \frac{D}{kT} Z^* e \rho j_y - \frac{D}{kT} Q^* \frac{1}{T} \frac{\partial T}{\partial y} - \frac{D}{kT} \Omega \frac{\partial \sigma_m}{\partial y}, \\
F_z &= \frac{D}{kT} Z^* e \rho j_z - \frac{D}{kT} Q^* \frac{1}{T} \frac{\partial T}{\partial z} - \frac{D}{kT} \Omega \frac{\partial \sigma_m}{\partial z}, \\
G(\xi_k, \eta_k, \zeta_k) &= \left(\frac{\partial \psi_i}{\partial x} F_x + \frac{\partial \psi_i}{\partial y} F_y + \frac{\partial \psi_i}{\partial z} F_z \right) \psi_j, \\
H(\xi_k, \eta_k, \zeta_k) &= D \left(\frac{\partial \psi_i}{\partial x} \cdot \frac{\partial \psi_j}{\partial x} + \frac{\partial \psi_i}{\partial y} \cdot \frac{\partial \psi_j}{\partial y} + \frac{\partial \psi_i}{\partial z} \cdot \frac{\partial \psi_j}{\partial z} \right).
\end{aligned}$$

The most commonly used local iteration scheme for solving the above equation is the α -family of approximation method in which a weighted average of the time derivatives at two consecutive time steps is approximated by linear interpolation of the values of the variable at two steps:

$$(3.6) \quad (1 - \alpha) \dot{c}_{t_i} + \alpha \dot{c}_{t_{i+1}} = \frac{c_{t_{i+1}} - c_{t_i}}{\Delta t}, \quad \text{for } 0 \leq \alpha \leq 1.$$

In this work, $\alpha = 0.5$ is used. Such method is called the Crank-Nicolson scheme which is stable and has the accuracy order of $O((\Delta t)^2)$ [12].

It follows from Eqs. (3.3) and (3.5) with considering the incremental step that

$$(3.7) \quad ([\mathbf{M}] + \alpha \Delta t [\mathbf{K}]) \{c_{t_{i+1}}\} = ([\mathbf{M}] - (1 - \alpha) \Delta t [\mathbf{K}]) \{c_{t_i}\} + \{\bar{\mathbf{Y}}\}_{i,i+1},$$

where

$$(3.8) \quad \{\bar{\mathbf{Y}}\}_{i,i+1} = (1 - \alpha) \Delta t \{\bar{\mathbf{Y}}\}_{t_i} + \alpha \Delta t [\mathbf{M}] \{\bar{\mathbf{Y}}\}_{t_{i+1}}.$$

Thus, the normalized atomic density c in the $(i+1)^{\text{th}}$ step can be obtained based on Eq. (3.6) in terms of the corresponding value in the i -th step. Since the initial atomic density $c_0 = 1$ is known, the above equations provide the solution to c at any time step. In this paper, the blocking boundary condition ($\mathbf{q} \cdot \mathbf{n} = 0$) is considered so $\{\bar{\mathbf{Y}}\}_{i,i+1} = \{0\}$.

3.2. Simulation approach of EM induced void evolution

The damage induced by electromigration appears as voids. Lifetime and failure location in a solder bump can be predicted by means of numerical simulation of the process of void incubation, initiation and growth. The changes in current density and temperature distribution due to void growth should be taken into account in simulation.

The computation procedure of EM induced void evolution based on ADI algorithm is shown in Fig. 1. The calculation consists of an incubation period and a growth period for a void. In the simulation for the incubation period, at first, the initial distributions of current density and temperature in the solder joint are obtained by 3D finite element method analysis based on ANSYS. Then, atom density redistribution in the considered solder bump is solved based on the ADI algorithm using a user-defined FORTRAN code. The data exchange between the ANSYS and FORTRAN codes is developed with ANSYS program design language (APDL) and the system batch language in Windows to transfer the data.

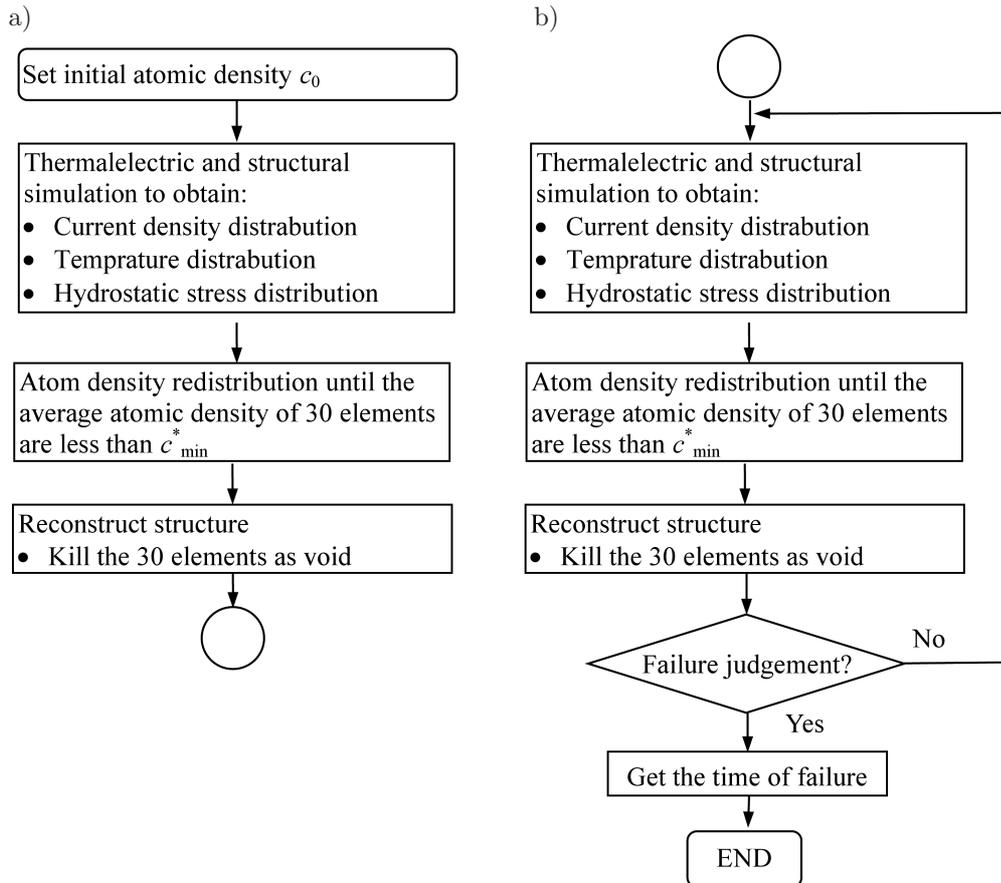


FIG. 1. Computational procedure for numerical simulation of the EM evolution: a) incubation period, b) void growth period.

We assume that there is a critical atomic density for void initiation c_{min}^* . When c is less than or equal to c_{min}^* ($c \leq c_{min}^*$), the void will appear or grow.

Conversely, when the normalized atomic density c is greater than or equal to c_{\max}^* ($c \geq c_{\max}^*$), a hillock will be generated. The values of c_{\min}^* can be obtained from experiments. The criterion we cited here is based on test data [13], for solder alloys $c_{\min}^* = 0.85$. In addition, the work in this paper can show the location of hillock, but it has not yet considered the formation of a hillock. In the simulation procedure of the void growth period, once the average atomic density value of the elements is less than the critical atomic density for void initiation c_{\min}^* , the corresponding elements will be killed (“element death”) and the structure, presented in Fig. 2, needs to be reconstructed. To achieve the “element death” effect, ANSYS does not actually remove “killed” elements. Instead, it deactivates them by reducing the element material attribute, such as the elastic modulus and resistivity, by a factor of $1.0E-6$.



FIG. 2. Schematic process flow of void evolution.

In the semiconductor industry for a FCBGA solder bump failure criterion, a 15% increment in electrical resistance of the bump is usually considered EM failure. This criterion is used in this paper to get the final TTF.

4. ELECTROMIGRATION SIMULATION RESULTS

A FCBGA package is chosen for the analysis in this paper, which includes Si die, solder bump, TIM, adhesive, underfill, stiffener ring, heat spreader, substrate, solder mask and PCB. Figure 3 is the cross-section of the package. The solder bump under this simulation connects the Si die to the package substrate. Because the structure of package is very complex, sub-model technique in

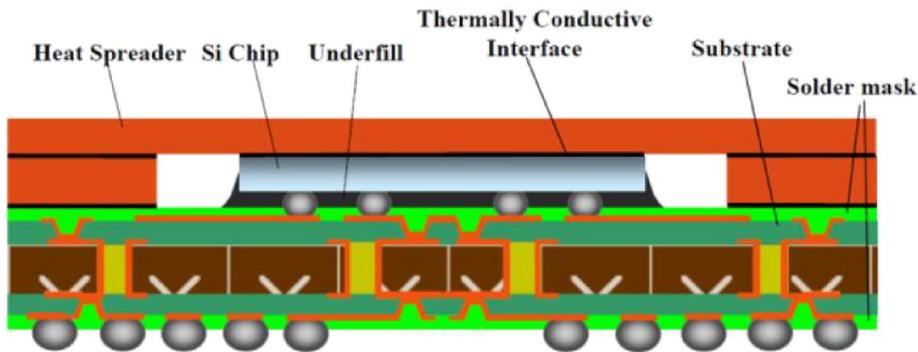


FIG. 3. FCBGA package.

ANSYS is introduced to get the better simulation results. Due to the symmetry of the package, the quarter model is built as the global model, as presented in Fig. 4a. In the first step, the global structure is modeled using relative coarse elements firstly. Then, a refined sub-model which is cut out from the global model is constructed as shown in Fig. 4b. This sub-model includes the solder bump of V1 in which the void is detected according to the electromigration test. The solder bump material is eutectic 63Sn-37Pb. All materials and their thermal, mechanical and electrical properties were taken from the literature [14].

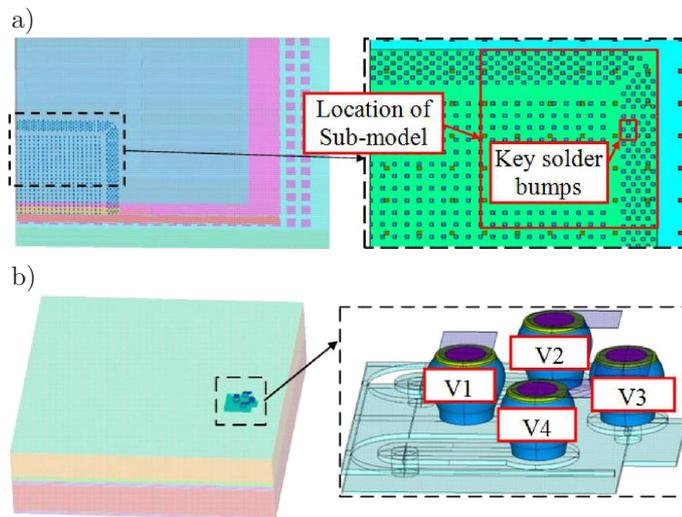


FIG. 4. a) global model of FCBGA package b) sub-model of FCBGA package.

In thermal-electrical analysis, the power dissipation of chip is 22 W. The ambient temperature is 32°C , and the convection boundary condition is applied in heat spreader and package exterior with the film coefficient of $7.25 \text{ W}/(\text{m}^2 \cdot ^{\circ}\text{C})$ and $6.8 \text{ W}/(\text{m}^2 \cdot ^{\circ}\text{C})$ respectively. Figure 5 shows the electron flow direction in sub-model.

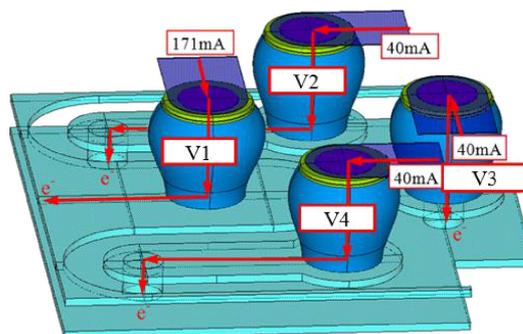


FIG. 5. Electron flow direction in sub-model.

Figure 6 shows the temperature distribution of global model, and the highest temperature is 75.6°C (the real temperature tested at the location is 75.5°C) at the chip. The displacement distribution of global model is shown in Fig. 7. Due to the anisotropic material of PCB (the CTE in Z direction is about four-five times in X/Y direction), the displacement in Z direction is much greater than the displacement in X and Y directions.

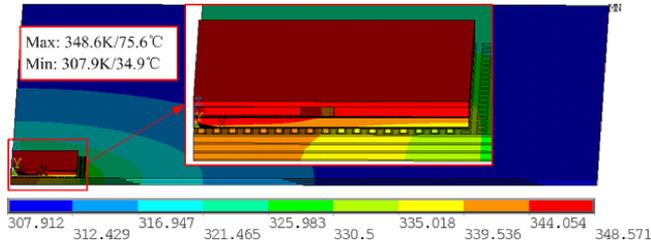


FIG. 6. Temperature distribution of global model.

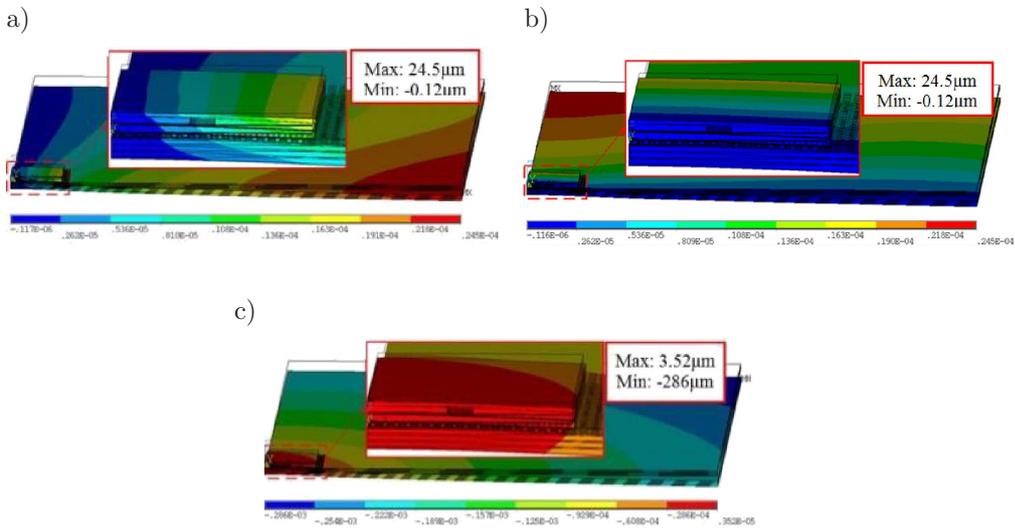


FIG. 7. Displacement distribution of global model: a) X direction, b) Y direction, c) Z direction.

The current crowding, which occurs when there is a sudden change in the cross-section area, is the main cause for the electromigration. Figure 8a shows the current density distribution in the V1 solder bump with the existing line-to-bump geometry design. As seen in this figure the current crowding occurs at the nearest corner at which a large portion of the current leaves the solder bump. The current density at the corner is approximately one order of the magnitude higher than the average current density in solder bumps.

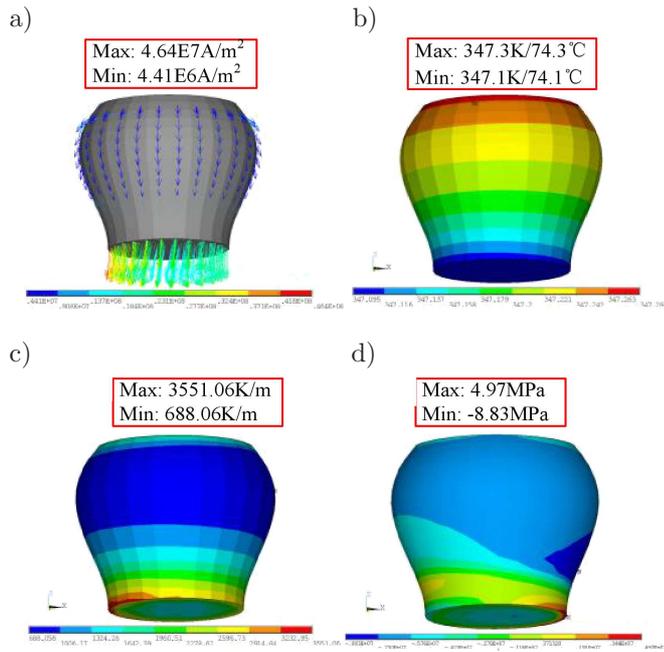


FIG. 8. Distribution of corresponding electrical-thermal-structural results of solder bump V1: a) current density distribution, b) temperature distribution, c) temperature gradient distribution, d) hydrostatical stress distribution.

A correlation of the simulated results and the experimental test results for V1 solder bump is presented in Fig. 9. It is observed that the void by simulation appears at the bottom of V1 solder bump which is similar to the void and failure mode shown in the test.

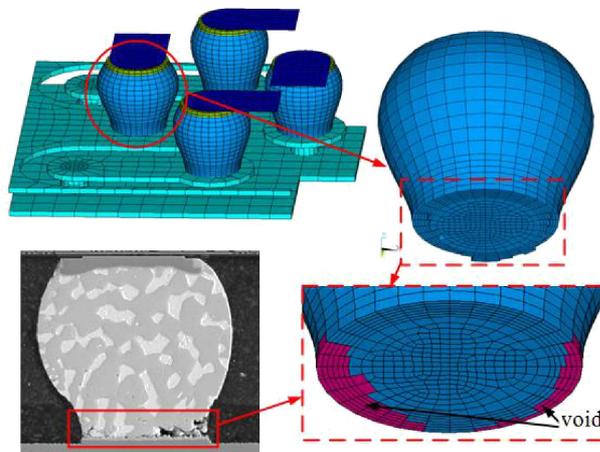


FIG. 9. Void formation between simulation solutions and test results.

5. DESIGN AND ANALYSIS BASED ON ORTHOGONAL EXPERIMENT DESIGN

Orthogonal experimental design is an experimental design method that studies multi-factor and multilevel. It selects test points, arranges experiments and analyses experimental data utilizing orthogonal table, then it ascertains primary and secondary parameters and interactive relationship, finally gets optimal combination of level. In this paper, orthogonal experimental design is used to evaluate the effect of design parameter on TTF. The design parameters for FCBGA package include: diameter of UBM, bottom diameter of solder bump, thickness of heat spreader and width of stiffener ring. Every design parameter gives three factor levels. Table 1 and Fig. 10 give the factor levels and schematic diagram of design parameters respectively.

Table 1. Design parameters.

Type of factors	Number	Factor levels		
		1	2	3
Diameter of UBM [mm]	A	0.095	0.1	0.11
Bottom diameter of solder bump [mm]	B	0.1	0.11	0.115
Thickness of heat spreader [mm]	C	0.38	0.46	0.54
Width of stiffener ring [mm]	D	5	8	11

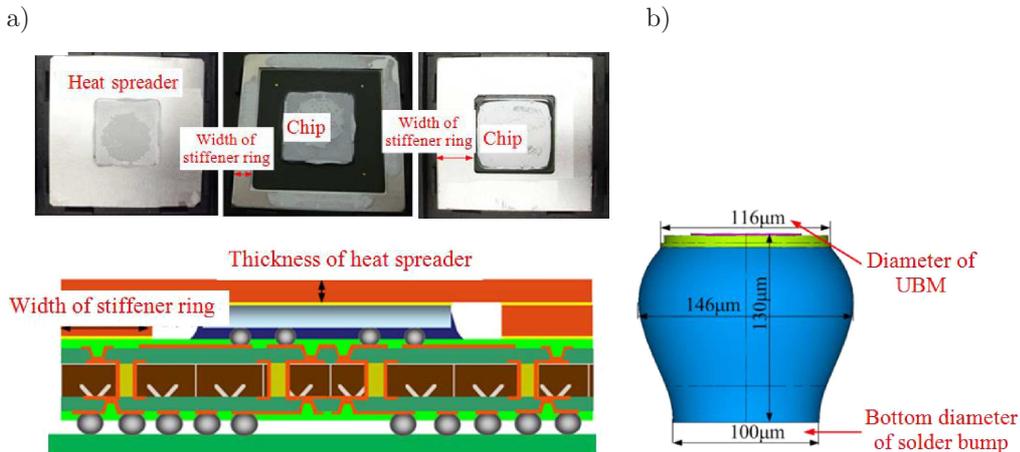


FIG. 10. Schematic diagram of design parameters: a) thickness of heat spreader and width of stiffener ring, b) diameter of UBM and bottom diameter of solder bump.

After experimental factors were determined, the appropriate orthogonal table was selected according to the number and level of the factor and the interaction

be considered. This work is a three-level and four-factor experiment. Table 2 lists the orthogonal array according to the design parameter in Table 1.

Table 2. Orthogonal array $L_9 (3^4)$.

Test No.	A	B	C	D	Scheme
1	1	1	1	1	$A_1B_1C_1D_1$
2	1	2	2	2	$A_1B_2C_2D_2$
3	1	3	3	3	$A_1B_3C_3D_3$
4	2	1	2	3	$A_2B_1C_2D_3$
5	2	2	3	1	$A_2B_2C_3D_1$
6	2	3	1	2	$A_2B_3C_1D_2$
7	3	1	3	2	$A_3B_1C_3D_2$
8	3	2	1	3	$A_3B_2C_1D_3$
9	3	3	2	1	$A_3B_3C_2D_1$

Electromigration simulations of FCBGA package are performed using different parameter value according to the scheme of Table 2, and the TTF with different design parameter is listed in Table 3. It shows that test no. 3 gets the longest TTF and test no. 1 gets the shortest TTF.

Table 3. TTF results of the experiment.

Test No.	A [mm]	B [mm]	C [mm]	D [mm]	TTF [h]	Rank
1	0.095	0.1	0.38	5	4.15×10^6	9
2	0.095	0.11	0.46	8	8.12×10^6	4
3	0.095	0.115	0.54	11	1.02×10^7	1
4	0.1	0.1	0.46	11	6.51×10^6	5
5	0.1	0.11	0.54	5	5.39×10^6	8
6	0.1	0.115	0.38	8	9.78×10^6	2
7	0.11	0.1	0.54	8	6.30×10^6	7
8	0.11	0.11	0.38	11	8.55×10^6	3
9	0.11	0.115	0.46	5	6.46×10^6	6

Figures 11 and 12 show the distributions of current density, temperature gradient and hydrostatical stress of V1 solder bump for test no. 1 and test no. 3 respectively. It can be seen that they have similar distribution of current density but very different temperature gradient and hydrostatical stress. The maximum of hydrostatical stress in test no. 1 is 38.9 MPa, which is 10 times the value

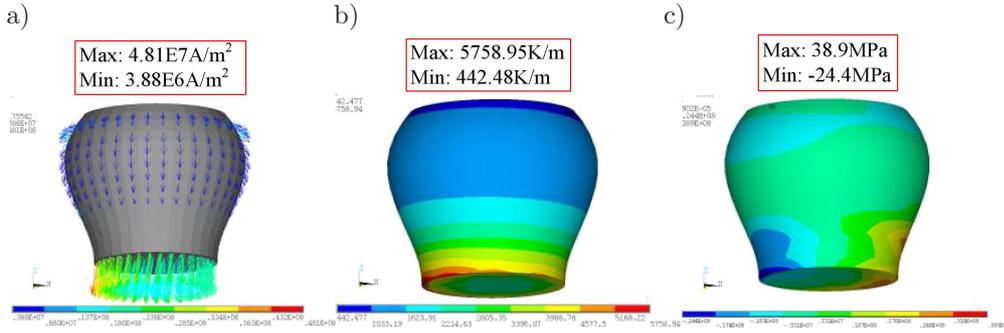


FIG. 11. Distribution of corresponding electrical-thermal-structural results for test no. 1:
 a) current density, b) temperature gradient, c) hydrostatical stress.

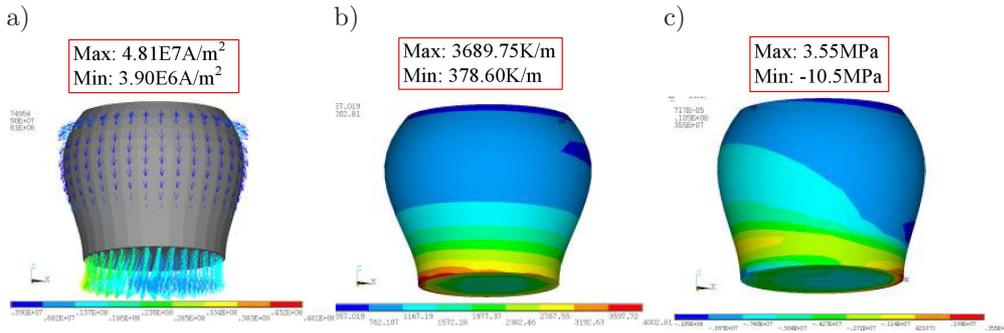


FIG. 12. Distribution of corresponding electrical-thermal-structural results for test no. 3:
 a) current density, b) temperature gradient, c) hydrostatical stress.

in test no. 3. From Table 4, we also can see that test no. 1 produces more displacement in Z direction than test no. 3. All these explain why test no. 1 gets shorter TTF than test no. 3.

Table 4. Displacement results of the experiment.

Test No.	UX [μm]		UY [μm]		UZ [μm]	
	Min	Max	Min	Max	Min	Max
1	-0.10	23.81	-0.09	23.79	-285	3.49
2	-0.10	24.18	-0.09	24.16	-276	3.49
3	-0.17	24.40	-0.17	24.38	-267	3.74
4	-0.12	24.50	-0.12	24.50	-286	3.52
5	-0.07	23.73	-0.07	23.71	-282	3.62
6	-0.10	24.22	-0.10	24.20	-276	3.43
7	-0.10	24.14	-0.09	24.12	-274	3.55
8	-0.14	24.48	-0.14	24.46	-269	3.53
9	-0.09	23.77	-0.08	23.74	-284	3.56

From Table 3, we can see that test no. 4 and test no. 9 have similar TTF even though they have very different structure dimension. According to Table 4, it can also be observed that the displacement of global model of test no. 4 is close to test no. 9. Therefore, the displacement of global model can reflect the TTF of solder bump. But it does not mean that more displacement will lead to shorter TTF.

6. EVALUATION OF ORTHOGONAL EXPERIMENTAL DESIGN

Currently, the most common method used in the analysis of the result of orthogonal experiment mainly include two types. One is the analysis of range and the other is the analysis of variance. In this paper, the analysis of range is used to analyse the effect of different factors on electromigration of solder bump, to evaluate the primary factors, and then to provide the optimal scheme. Through the analysis of the range R_j (see Eq. (6.1)), we come to conclusion with excellent level of different factors. The bigger R_j is, the higher the optimal level of the factor becomes.

$$(6.1) \quad R_j = \max [\bar{y}_{j1}, \bar{y}_{j2}, \dots, \bar{y}_{jk}] - \min [\bar{y}_{j1}, \bar{y}_{j2}, \dots, \bar{y}_{jk}],$$

$$(6.2) \quad y_{jk} = \sum_{k=1}^n |eve|_{jk},$$

where y_{jk} shows that each column of orthogonal table has experimental results at different levels, $\bar{y}_{jk} = y_{jk}/k$ is the average value of each row of different experimental results of orthogonal table.

According to Eqs. (6.1) and (6.2), the analysis result of orthogonal experiment is shown in Table 5. We make clear that the R value of B is the maximum,

Table 5. Analysis of range.

Factor	TTF (h)			
	A	B	C	D
y_1	2.25×10^7	1.70×10^7	2.25×10^7	1.60×10^7
y_2	2.19×10^7	2.21×10^7	2.11×10^7	2.42×10^7
y_3	2.13×10^7	2.64×10^7	2.19×10^7	2.53×10^7
\bar{y}_1	7.49×10^6	5.65×10^6	7.49×10^6	5.33×10^6
\bar{y}_2	7.23×10^6	7.35×10^6	7.03×10^6	8.07×10^6
\bar{y}_3	7.10×10^6	8.81×10^6	7.30×10^6	8.42×10^6
R	3.9×10^5	3.16×10^6	4.6×10^5	3.09×10^6
Results	B > D > C > A			

so we obtain the most important impacting factor of TTF is bottom diameter of solder bump, following are width of stiffener ring and thickness of heat spreader and the last one is diameter of UBM. Figure 13 shows the relationship between TTF and different factors. We can find that the TTF will increase while the bottom diameter of solder bump and width of stiffener ring increase. But as diameter of UBM increases, the TTF of solder bump will decrease.

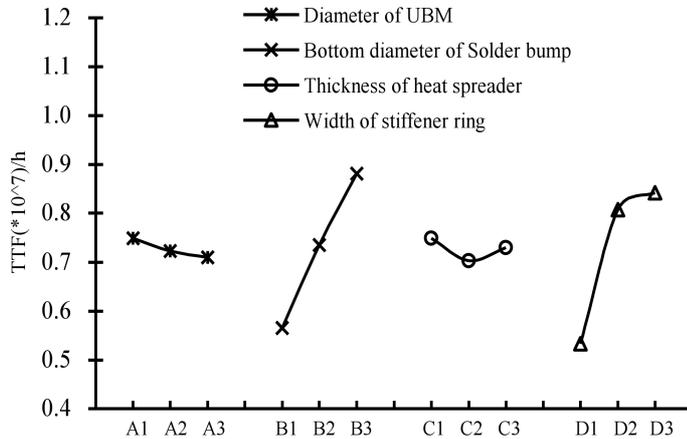


FIG. 13. Relationship between TTF and factors.

It can be concluded from Table 5 and Fig. 13 that the experimental optimal combination of level is $A_1B_3C_1D_3$, which is not included in orthogonal array of Table 2. As mentioned above, the optimal combination in Table 2 is $A_1B_3C_3D_3$. Next, we will compare the results of $A_1B_3C_1D_3$ and $A_1B_3C_3D_3$ combinations and investigate which is a better choice.

Figure 14 shows the distributions of electrical-thermal-structural results for $A_1B_3C_1D_3$ combination. Compared with Fig. 11, all results of current density,

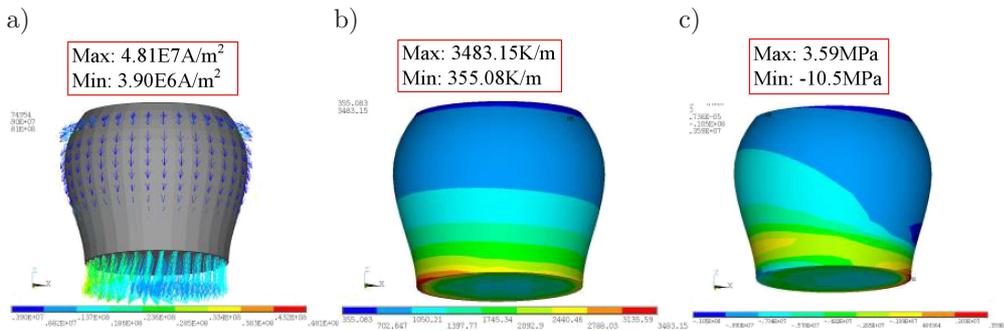


FIG. 14. Distribution of corresponding electrical-thermal-structural results for $A_1B_3C_1D_3$ combination: a) current density, b) temperature gradient, c) hydrostatical stress.

temperature gradient and hydrostatical stress are very similar. The TTF for $A_1B_3C_1D_3$ combination is also obtained, which is 1.04×10^7 h. It only increases 1.96% compared with $A_1B_3C_3D_3$ combination. But if $A_1B_3C_1D_3$ is used, the usage of material will be reduced by 30%.

7. CONCLUSION

The electromigration simulation is performed on FCBGA package based on ADI method, and the simulation results for void generation and TTF have a reasonably good correlation with the testing results. Orthogonal experimental design is used to evaluate the effect of design parameters on TTF. It is found that bottom diameter of solder bump has the most significant impact on TTF, following are width of stiffener ring, thickness of heat spreader and the last one is diameter of UBM

ACKNOWLEDGMENT

The supports from Zhejiang Provincial Natural Science Foundation (No. LQ13E050014) are greatly appreciated.

REFERENCES

1. WU J.D., LEE C.W., ZHENG P.J., LI S., *Effects of substrate metallization on the degradation of flip chip interconnects under electromigration*, [in:] Proc. 9th Inter. Symp. on Advanced Pack Materials: Processes, Properties and Interfaces, 25–30, 2004.
2. DANDU P., FAN X. J., LIU Y., DIAO C., *Finite element modeling on electromigration of solder joints in wafer level packages*, Microelectronics Reliability, **50**, 4, 547–555, 2010.
3. CERIC H., SELBERHERR S., *Electromigration in submicron interconnect features of integrated circuits*, MATER. SCI. ENG. R.: Reports, **71**, 5–6, 53–86, 2010.
4. BLACK J.R., *Mass transport of aluminum by momentum exchange with conducting electrons*, [in:] Proc. 6th Annual Reliab. Physics Symp., 148–159, 1967.
5. CERIC H., SELBERHERR S., *Electromigration in submicron interconnect features of integrated circuits*, MATER. SCI. ENG.R.: Reports, **71**, 5–6, 53–86, 2010.
6. LIANG S.W., CHANG Y.W., SHAO T.L., CHEN C., TU K.N., *Effect of three-dimensional current and temperature distributions on void formation and propagation in flip-chip solder joints*, Appl. Phys. Lett., **89**, 2, 021117, 2006.
7. NAH J.W., REN F., TU K.N., VENK S., CAMARA G., *Electromigration in Pb-free flip chip solder joints on flexible substrates*, J. Appl. Phys., **99**, 2, 023520, 2006.
8. TU K.N., *Recent advances on electromigration in very-large-scale integration of interconnects*, J. Appl. Phys., **94**, 9, 5451–5473, 2003.
9. GAN H., CHOI W.J., XU G., TU K.N., *Electromigration in solder joints and solder lines*, J. Miner. Met. Mater. Soc., **54**, 6, 34–37, 2002.

10. BASARAN C., LIN M., *Damage mechanics of electromigration induced failure*, Mech. Mater., **40**, 1–2, 66–79, 2008.
11. LIU Y., ZHANG Y.X., LIANG L.H., *Prediction of electromigration induced voids and time to failure for solder joint of a wafer level chip scale package*, IEEE T Compon Pack T, **33**, 3, 544–552, 2010.
12. LIU Y., *Power electronic packaging: design, assembly process, reliability and modeling*. Springer, New York, 2012.
13. REDDY J.N., *An introduction to the finite element method*, 3rd ed., McGraw-Hill, New York, 55–56, 2006.
14. HUANG J., TU K.N., GEE S., NGUYEN L., *The effect of electromigration on eutectic SnPb and Pb-Free solders in wafer level-chip scale packages*, Proc. Semiconductor Res. Corporation Tech. Con., Portland, Oregon, USA Oct 24–26, 2005.
15. LIANG L.H., ZHANG J. C., ZHANG Y.X., *Research of electromigration failure for FCBGA solder joint under the multi-physical field*, Eng. Mech., **30**, 9, 264–269, 2013.

Received January 8, 2015; accepted April 8, 2015.
